

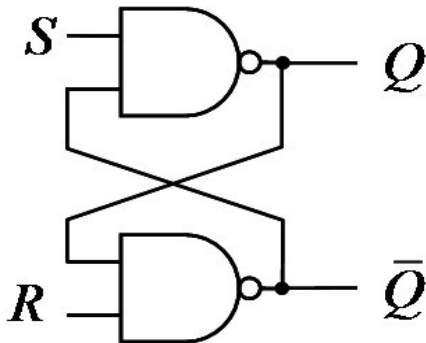
## SEQUENTIAL CIRCUITS

### FLIP-FLOPS

Flip Flops are binary storage elements come under the category of Sequential circuits. A flip flop stores a binary digit either 0 or 1. In otherwords, it has two stable states namely HIGH and LOW. HIGH state stores 1 and LOW state stores 0.

#### R-S Flip-flop:

The R-S flip-flop can be realized using NAND gates. The circuit diagram and the truth table of R-S flip-flop are shown below.



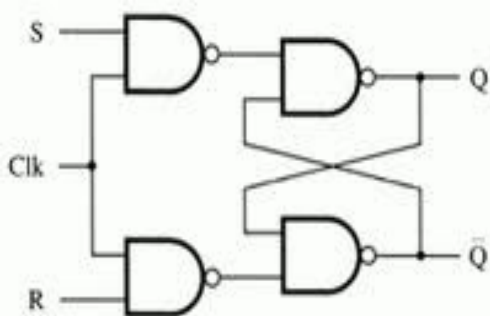
**Function Table**

R	S	Q	Comment
0	0	*	Race Condition
0	1	1	SET
1	0	0	RESET
1	1	Q'	Previous State

A 0 on any input to NAND gate will make its output high. Therefore when R=0 and S=0, the output of the flip-flop becomes unpredictable. This state is sometimes referred to as a *forbidden state* or *race condition*. When R=0 and S=1, the output Q of the flip-flop is set to 1. This state is called *set* state. When R=1 and S=0, the output Q of the flip-flop is reset to 0. This state is called *reset* state. When R=1 and S=1, the output Q of the flip-flop will remain in its previous state. In other words, the output of the flip-flop will not change.

#### Clocked R-S or S-R flip-flop:

The circuit diagram and the truth table of a S-R flip-flop are shown below.



**Function Table**

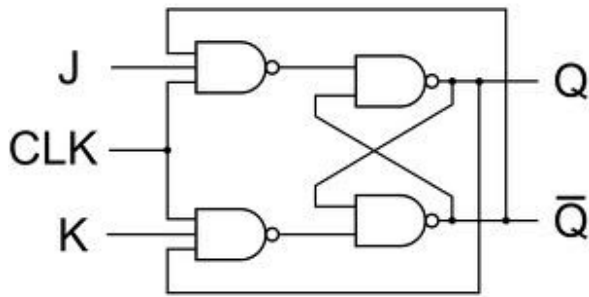
Clock	R	S	Q	Comment
0	X	X	NC	No change
1	0	0	NC	No Change
1	0	1	1	SET
1	1	0	0	RESET
1	1	1	*	Impredictable(Racing)

When the CLK input is 0, the output of the flip-flop will not change irrespective of the inputs at S and R. The flip-flop is disabled when the clock is 0. When the CLK input is 1, the output of the flip-flop will change according to the S and R inputs. The flip-flop is enabled when the clock is 1. The response of the flip-flop for various S and R inputs, when the CLK is 1, is as follows.

When R=0 and S=0, the output of the flip-flop will not change. When R=0 and S=1, the output Q of the flip-flop is set to 1. When R=1 and S=0, the output Q of the flip-flop is reset to 0. When R=1 and S=1, the output Q of the flip-flop becomes unpredictable.

### J-K flip-flop:

The circuit diagram and the truth table of a J-K flip-flop are shown below.



**Function Table**

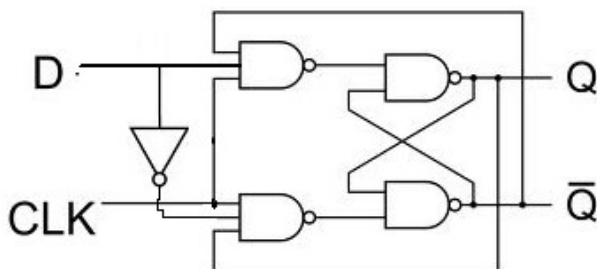
CLK	J	K	Q	Comment
0	X	X	NC	No Change
↑	0	0	NC	No Change
↑	0	1	0	RESET
↑	1	0	1	SET
↑	1	1	*	TOGGLE

When the CLK input is 0, the output of the flip-flop will not change irrespective of the inputs at J and K. The flip-flop is disabled when the clock is 0. When the CLK input is 1, the output of the flip-flop will change according to the J and K inputs. The flip-flop is enabled when the clock is 1. The response of the flip-flop for various J and K inputs, when the CLK is 1, is as follows.

When J=0 and K=0, the output of the flip-flop will not change. When J=0 and K=1, the output Q of the flip-flop is set to 1. When J=1 and K=0, the output Q of the flip-flop is reset to 0. When J=1 and K=1, the clock pulse switches the output of the flip-flop to its *complement* state. This state is also referred to as *toggle* state. There is no forbidden or unpredictable state in a J K flip-flop.

### D flip-flop:

The circuit diagram and the truth table of a D flip-flop are shown below.



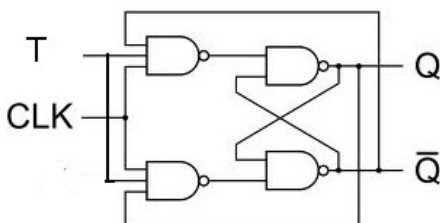
**Function Table**

CLK	D	Q	Comment
0	X	NC	No Change
↑	0	0	RESET
↑	1	1	SET

When the CLK input is 0, the output of the flip-flop will not change irrespective of the input D. The flip-flop is disabled when the clock is 0. When the CLK input is 1, the output of the flip-flop will change according to the D input. The flip-flop is enabled when the clock is 1. The response of the flip-flop for various D input, when the CLK is 1, is as follows. When D=0, the output Q of the flip-flop become 0 (reset). When D=1, the output Q of the flip-flop become 1 (set). There is no forbidden or unpredictable state in a D flip-flop. A D flip-flop is sometimes referred to as a *data* flip-flop.

### T flip-flop:

The circuit diagram and the truth table of a T flip-flop are shown below.



**Function Table**

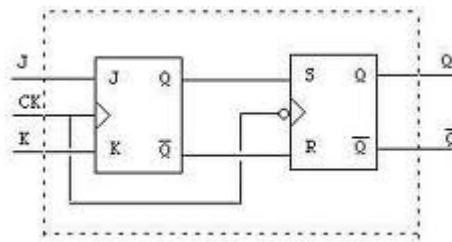
CLK	T	Q	Comment
0	X	NC	No Change
↑	0	NC	No Change
↑	1	1	Toggle

A T flip-flop can be realized from a J-K flip-flop when inputs J and K are combined to provide a single input designated as T. When the CLK input is 0, the output of the flip-flop will not change irrespective of the input T. The flip-flop is disabled when the clock is 0. When the CLK input is 1, the output of the flip-flop will change according to the T input. The flip-flop is enabled when the clock is 1.

The response of the flip-flop for various T input, when the CLK is 1, is as follows. When T=0, the output Q of the flip-flop will remain unchanged. When T=1, the clock pulse switches the output of the flip-flop to its complement (toggle) state. A T flip-flop is sometimes referred to as a *toggle* flip-flop.

**J-K Master-Slave Flip-flop:**

The circuit diagram of a J-K Master-Slave flip-flop is shown below.

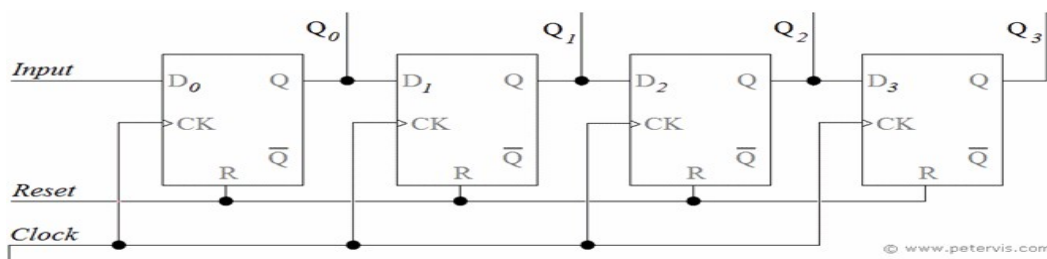


The circuit consists of two J-K flip-flops of which one is called the master and other the slave. The master flip-flop is positive-edge-triggered and the slave is negative-edge triggered. Therefore, the master responds to its J and K inputs before the slave. The master flip-flop changes state during the positive clock pulse and the slave changes state during the successive negative clock pulse.

If J = 1 and K = 0, the master sets on the positive clock edge. The high Q output of the master drives the J input of the slave. So, when the negative clock edge hits, the slave sets, copying the action of the master. If J = 0 and K = 1, the master resets on the positive clock edge. The high Q' output of the master drives the K input of the slave. Hence, the arrival of the negative clock edge forces the slave to reset. If the J and K inputs of the master are both high, it toggles on the positive clock edge and the slave then toggles on the negative clock edge. Regardless of what the master does, therefore, the slave copies it; if the master sets, the slave sets; if the master resets, the slave resets.

**SHIFT REGISTERS:**

A register is a group of flip-flops that can be used to store a binary word. There must be one flip-flop for each bit in the binary word. For instance, a register used to store an 8-bit word must have eight flip-flops. A register capable of shifting its binary information in one or both directions is called a shift register. The logical organization of a shift register consists of a chain of flip-flops in cascade, with the output of one flip-flop connected to the input of the next flip-flop. All flip-flops receive common clock pulses that initiate the shift from one stage to the next. The shift register that shifts bits towards right is called a shift right register and that which shifts towards left is called a shift left register. The circuit diagram of a 4-bit shift right register, constructed using J-K flip-flops, is shown in the figure below.



For a J-K flip-flop, the data bit to be shifted into the flip-flop must be present at the J and K inputs when the clock strikes. To shift a 0 into the flip-flop,  $J = 0$  and  $K = 1$ . To shift a 1 into the flip-flop,  $J = 1$  and  $K = 0$ . The circuit consists of four J-K flip-flops, whose outputs are designated as A, B, C, and D. The data bits to be shifted are given at the J and K inputs of flip-flop A. The outputs of flip-flop A is connected to the inputs of flip-flop B. The outputs of flip-flop B is connected to the inputs of flip-flop C and so on. The clock pulse is connected to all the flip-flops as shown in the figure.

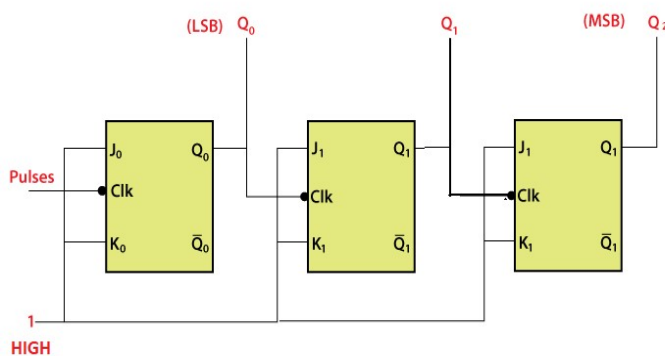
Consider the data bits at the inputs of flip-flop A as  $J = 1$ , and  $K = 0$ . As the clock pulses are applied to all the flip-flops directly, each flip-flop changes state depending on its J and K inputs at the time of arrival of the clock pulse. When the first clock pulse strikes, the 0 in C is shifted into D, the 0 in B is shifted into C, the 0 in A is shifted into B and the data input 1 is shifted into A. At this point of time the output  $ABCD = 1000$ . When the second clock pulse strikes, the 0 in C is shifted into D, the 0 in B is shifted into C, the 1 in A is shifted into B and the data input 1 is shifted into A. The output at this stage is  $ABCD = 1100$ . The shifting continues in this order for every strike of the clock pulse and at the end of the fourth clock pulse the outputs of the flip-flops would be  $ABCD = 1111$ . This is illustrated in the table given above.

## COUNTERS

Counters are Sequential Circuits used to count number of electrical pulses. Since a counter that follows the binary number sequence, it is called a binary counter. An n-bit counter consists of n flip-flops and can count in binary from 0 through  $2^n - 1$ . There are basically two types of counters – asynchronous and synchronous counters.

### Asynchronous Counter

In an asynchronous counter, each flip-flop is triggered by the previous flip-flop. In other words, the output of a flip-flop is used as the clock input for the next flip-flop. Such a counter is also called a ripple counter or a serial counter. A 3-bit binary ripple counter can be constructed using three JK flip-flops as shown in the figure below:



Clock	C	A	B
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

The system clock drives flip-flop A. The output of flip-flop A drives flip-flop B, and the output of flip-flop B drives flip-flop C. All the J and K inputs are connected to  $+V_{cc}$ . This means each flip-flop will change state with a negative transition of the clock input.

To understand the operation of this counter, refer to the functional table given above. The count starts with 000 and increments by one with each clock pulse input. After the count 111, the counter goes back to 000 to repeat the count. The least significant bit A is complemented with each clock pulse input. Every time A goes from 1 to 0, it complements B. Every time B goes from 1 to 0, it complements C, and so on for any other higher order bits of a counter.

A counter with three flip-flops is often referred to as a modulus-8 (or mod-8) counter since it counts 8 states. Similarly, a counter with four flip-flops is called a mod-16 counter, and so on. The modulus of a counter is the total number of states through which the counter can progress.

## Ripple Counter

Ripple counter is a special type of **Asynchronous** counter in which the clock pulse ripples through the circuit. The n-MOD ripple counter forms by combining n number of flip-flops. The n-MOD ripple counter can count  $2^n$  states, and then the counter resets to its initial value.

### Features of the Ripple Counter:

- Different types of flip flops with different clock pulse are used.
- It is an example of an asynchronous counter.
- The flip flops are used in toggle mode.
- The external clock pulse is applied to only one flip flop. The output of this flip flop is treated as a clock pulse for the next flip flop.
- In counting sequence, the flip flop in which external clock pulse is passed, act as LSB.

### *Synchronous Counter:*

Synchronous counters are different from ripple counters in that clock pulses are applied to all the flip-flops directly. A common clock triggers all the flip-flops simultaneously. The decision whether a flip-flop is to be complemented or not is determined from the values of the data inputs J and K at the time of the clock pulse. If  $J = K = 0$ , the flip-flop does not change state. If  $J = K = 1$ , the flip-flop toggles.

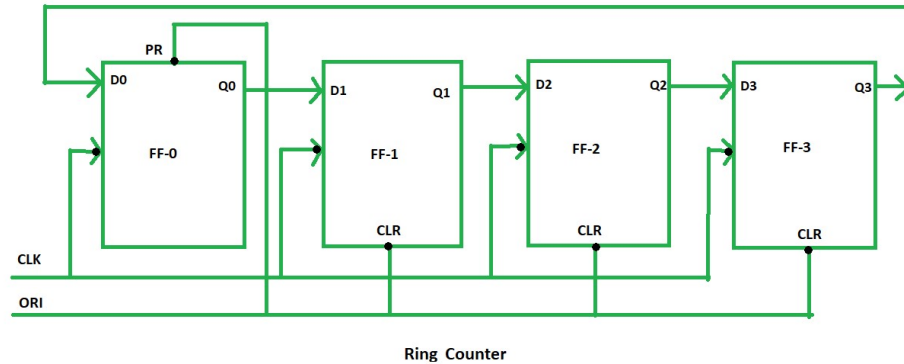
In a synchronous binary counter, the flip-flop in the least significant position is complemented with every clock pulse. A flip-flop in any other position is complemented when all the bits in the lower significant positions are equal to 1. The circuit diagram and the functional table of a 3-bit synchronous counter is shown in the figure below.

The clock inputs of all the flip-flops are connected to a common clock. The counter is enabled with the count enable input ( $+V_{cc}$ ). The first stage flip-flop A has its J and K inputs equal to 1. The J and K inputs of other flip-flops are equal to 1 if all previous least significant stages are equal to 1 and the count is enabled. The chain of AND gates generates the required logic for the J and K inputs in each stage. For example, if the present state of the counter is  $CBA = 0011$ , the next count is 100. A is always complemented. B is complemented because the present state of  $A = 1$ . C is complemented because the present state of  $BA = 11$ . The counter can be extended to any number of stages, with each stage having an additional flip-flop and an AND gate that gives an output of 1 if all previous flip-flop outputs are 1.

## RING COUNTER

A ring counter is constructed by connecting the outputs of the last flip-flop of the shift register to the inputs of the first flip-flop. The circuit diagram of a 4-bit ring counter is shown in the figure below.

Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
repeat			



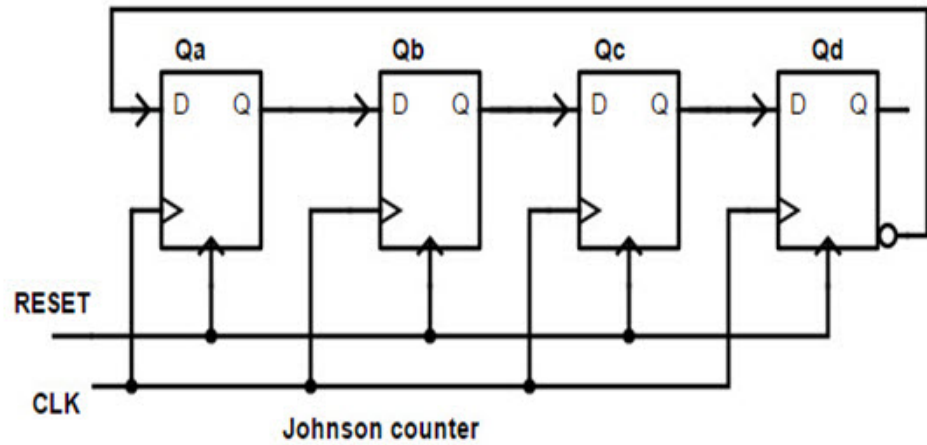
The outputs of the flip-flop A is connected to the inputs of flip-flop B. The outputs of the flip-flop B is connected to the inputs of flip-flop C. The outputs of the flip-flop C is connected to the inputs of flip-flop D. The outputs of the flip-flop D is fed back and connected to the inputs of flip-flop A. The clock pulse is connected to all the flip-flops directly. When the clock pulse is allowed to run, the outputs of all the flip-flops will never change, as long as the low output of flip-flop D is connected to the input of A.

Suppose that, by some external means, flip-flop A is made high, and all other flip-flops are low, and then the clock is allowed to run. During the first clock pulse, the 1 in flip-flop A will shift into flip-flop B and flip-flop A will be reset (0), since the 0 in flip-flop D will shift into flip-flop A. All other flip-flops will still contain 0s. The second clock pulse will shift the 1 in flip-flop B into flip-flop C, while B resets. The third clock pulse will shift the 1 in flip-flop C into flip-flop D, and so on. Thus the single 1 will shift down the register, traveling from one flip-flop to the next flip-flop for each clock pulse. When it reaches flip-flop D, the next clock will shift it into flip-flop A by means of the feedback connection. This configuration is also referred to as a circulating register. The following table shows the state of the ring counter for each clock pulse.

## JOHNSON COUNTER (SHIFT COUNTER)

This counter is constructed by crossing the outputs of the last flip-flop and connecting them to the inputs of the first flip-flop. This type of feedback is called inverse feedback. The circuit diagram of the Johnson counter is shown in the figure below. The output D is connected to the K input of A, and D' is connected to the J input of A.

Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
repeat			



Now assume that all flip-flops are in reset condition and the clock is allowed to run. Since D' is high and D is low, a 1 is set in flip-flop A during the first clock pulse. At the same time, B and C remain low since their J inputs are low and their K inputs are high. During the second clock pulse, A remains high since D' is still high and D is still low. At the same time, B is set high since A is now high and A' is low; C remains unchanged since B is low during this period. During the third clock pulse, A and B remain high and C is set high since B is now high. During the fourth clock pulse, A, B and C remain high and D is set high since C is now high. Thus after four clock cycles, all the four flip-flops have been changed from the 0 state to the 1 state.

During the fifth clock pulse, D is high and D' is low; therefore, A is reset to the low state, and B, C and D remain high. During the sixth clock pulse, A remains low, B is reset to low (since A is now low and A' is high), C and D remains high. During the seventh clock pulse, A and B remains low, C is reset to low, and D remains high. During the eighth clock pulse, A, B, C remains low and D is reset to low. The counter returns to the initial start state 0000. Thus this shift register with inverse feedback has progressed through a complete cycle of counts in 8 clock cycles. This counter is also referred to as a shift counter. The truth table of a 4-bit shift counter is given below.

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